

## CLAIMS

What is claimed is:

- 1           1.       An integrated circuit comprising:  
2           clock generation circuitry to generate a master clock signal and at least one  
3           other clock signal transmitted through a clock distribution tree to a circuit component,  
4           the circuit component receiving the master clock signal at a first component block; and  
5           bypass logic to define a bypass path to allow a second component block of the  
6           circuit component to receive the master clock signal, wherein the first and second  
7           components are controlled by a common clock domain in response to the master clock  
8           signal.
- 1           2.       The integrated circuit of claim 1, wherein the bypass logic includes a  
2           switch that allows for the coupling of either the master clock signal or the other clock  
3           signal to the second component block of the circuit component.
- 1           3.       The integrated circuit of claim 2, wherein the switch is responsive to a  
2           master select signal to select the master clock signal for coupling to the second  
3           component block of the circuit component.
- 1           4.       The integrated circuit of claim 1, wherein the bypass logic includes a  
2           bypass switch located in the second component block of the circuit component.
- 1           5.       The integrated circuit of claim 4, wherein the bypass switch is  
2           responsive to a bypass activation signal to activate the bypass path.
- 1           6.       The integrated circuit of claim 1, further comprising a default path to  
2           allow the second component block of the circuit component to receive the other clock  
3           signal such that the clock domain of the second component block of the circuit  
4           component is different from the clock domain of the first component block of the  
5           circuit component.
- 1           7.       The integrated circuit of claim 6, wherein the default path is  
2           automatically selected when the integrated circuit powers up.

1           8.     The integrated circuit of claim 7, wherein the bypass path is selected by  
2 a user.

1           9.     The integrated circuit of claim 8, wherein selecting the bypass path  
2 further includes utilizing software to write a bit to a clocking register to instruct the  
3 circuit component to use the bypass path.

1           10.    A method comprising:  
2           designing a plurality of circuit components on an integrated circuit that achieve  
3 a clock skew less than a predetermined minimum;  
4           designing a clock distribution tree for the plurality of circuit components on the  
5 integrated circuit to achieve the clock skew across all combinable circuit components  
6 and component blocks of the circuit components; and  
7           for at least one of the plurality of circuit components,  
8           defining two signal paths:  
9                   a default path; and  
10                  a bypass path.

1           11.    The method of claim 10, wherein the at least one circuit component  
2 includes a first component block and a second component block, further comprising:  
3           clocking the first component with a master clock signal; and  
4           clocking the second component block with a circuit component clock  
5 signal.

1           12.    The method of claim 11, wherein the bypass path allows the second  
2 component block to receive the master clock signal such that a clock domain of the  
3 second component block of the at least one circuit component is the same as a clock  
4 domain of the first component block of the at least one circuit component.

1           13.    The method of claim 12, wherein the bypass path includes bypass logic  
2 having a bypass switch located in the second component block of the at least one circuit  
3 component.

1           14.     The method of claim 13, wherein the bypass switch is responsive to a  
2     bypass activation signal to activate the bypass path.

1           15.     The method of claim 11, wherein the default path allows the second  
2     component block of the at least one circuit component to receive the circuit component  
3     clock signal such that the clock domain of the second component block of the circuit  
4     component is different from the clock domain of the first component block of the  
5     circuit component.

1           16.     The method of claim 15, wherein the default path is automatically  
2     selected when the integrated circuit powers up.

1           17.     The method of claim 11, further comprising determining if the  
2     integrated circuit is functional, if not,  
3                 selecting the bypass path.

1           18.     The method of claim 17, wherein selecting the bypass path further  
2     includes utilizing software to write a bit to a clocking register to instruct the at least one  
3     circuit component to use the bypass path.

1           19.     The method of claim 11, wherein the bypass path is selected by a user.

1           20.     A system comprising:  
2             a processor coupled to memory; and  
3             an integrated circuit coupled to the processor, the integrated circuit including:

4                 clock generation circuitry to generate a master clock signal and at least  
5             one other clock signal transmitted through a clock distribution tree to a circuit  
6             component, the circuit component receiving the master clock signal at a first  
7             component block; and

8                 bypass logic to define a bypass path to allow a second component block  
9             of the circuit component to receive the master clock signal, wherein the first and  
10            second components are controlled by a common clock domain in response to  
11            the master clock signal.

1           21.     The system of claim 20, wherein the bypass logic includes a switch that  
2 allows for the coupling of either the master clock signal or the other clock signal to the  
3 second component block of the circuit component.

1           22.     The system of claim 21, wherein the switch is responsive to a master  
2 select signal to select the master clock signal for coupling to the second component  
3 block of the circuit component.

1           23.     The system of claim 20, wherein the bypass logic includes a bypass  
2 switch located in the second component block of the circuit component.

1           24.     The system of claim 23, wherein the bypass switch is responsive to a  
2 bypass activation signal to activate the bypass path.

1           25.     The system of claim 20, further comprising a default path to allow the  
2 second component block of the circuit component to receive the other clock signal such  
3 that the clock domain of the second component block of the circuit component is  
4 different from the clock domain of the first component block of the circuit component.

1           26.     The system of claim 25, wherein the default path is automatically  
2 selected when the integrated circuit powers up.

1           27.     The system of claim 26, wherein the bypass path is selected by a user.

1           28.     The system of claim 27, wherein selecting the bypass path further  
2 includes, the processor utilizing software stored in memory to write a bit to a clocking  
3 register to instruct the circuit component to use the bypass path.